IN THE CLAIMS:

1. (original) A verification system comprising:

a representation of a first design representing a specification having a predetermined functionality;

a representation of a second design, the representation of the second design intended to satisfy the predetermined functionality of the first design, the verification system functioning to affirm that the representation of the second design satisfies the predetermined functionality of the representation of the first design;

a plurality of design inputs;

a tester for comparing the representation of the second design with the representation of the first design, and detecting when the representation of the second design does not satisfy the representation of the first design, the tester providing a failure indicator and a characterization of a failure in response to the detecting, the tester further comprising:

a failure analyzer for applying one or more constraints to the characterization of the failure, the one or more constraints representing restrictions on permissible test parameters of the second design representation, and determining whether the one or more constraints will prevent the failure from occurring.

2. (original) The verification system of claim 1 wherein the verification system functions to affirm that the second design is fully functionally equivalent to the first design.

3. (original) The verification system of claim 1 wherein one of the first design or the second design is an RTL representation and the other is a gate level representation.

4. (original) The verification system of claim 1 wherein one of the first design or the second design is an RTL representation and the other is a transistor level representation.

5. (original) The verification system of claim 1 wherein the representation of the first design and the representation of the second design are two different representations of a same design.

6. (original) The verification system of claim 1 wherein the constraints are supplied as design inputs.

7. (original) The verification system of claim 1 wherein the constraints are supplied by a user of the verification system.

8. (original) The verification system of claim 1 wherein the constraints originate from the tester.

9. (previously presented) The verification system of claim 1 wherein the first design and the second design represent a portion of an integrated circuit design that is less than all of the integrated circuit design, and wherein another portion of the integrated circuit design at least partially determines the one or more constraints.

10. (original) The verification system of claim 1 wherein the one or more constraints further comprise a set of constraints, and an order in which the set of constraints is applied is dependent upon the characterization of the failure.

11. (original) The verification system of claim 10 wherein not every constraint within the set of constraints is applied to the characterization of the failure.

12. (original) The verification system of claim 1 wherein the one or more constraints are generated by any of the following comprising:

(a) creation of cutpoints in the representation of the first design and the representation of the second design;

(b) input signals external to the representation of the first design and the representation of the second design; or

(c) state-holding elements contained within the representation of the first design and the representation of the second design.

13. (original) A method of verifying functional similarity between a first design and a second design intended to satisfy functionality of the first design, comprising:

receiving a representation of the first design;

receiving a representation of the second design;

receiving a plurality of design inputs;

executing a test program on a computer that compares the representation of the second design with the representation of the first design, and detecting when the representation of the second design does not satisfy the representation of the first design, the test program providing a failure indicator and a characterization of a failure in response to the detecting, the test program further comprising:

applying one or more constraints to the characterization of the failure, the one or more constraints representing restrictions on permissible test parameters of the second design representation, and analyzing the failure by determining whether the one or more constraints will prevent the failure from occurring.

14. (original) The method of claim 13 further comprising:

affirming that the second design is fully functionally equivalent to the first design.

15. (original) The method of claim 13 further comprising:

obtaining the one or more constraints that are applied to the characterization of the failure as a portion of the plurality of design inputs that are received.

16. (previously presented) The method of claim 13 further comprising:

permitting another design separate from the first design and the second design to at least partially determine the one or more constraints.

17. (original) The method of claim 13 further comprising:

creating a set of constraints, and applying predetermined ones of the set of constraints in an order that is dependent upon the characterization of the failure.

18. (original) The method of claim 13 further comprising:

generating the one or more constraints by having constraints associated with any of the following comprising:

cutpoints created in the representation of the first design and the representation of the second design, input signals external to the representation of the first design and the representation of the second design, or state-holding elements contained within the representation of the first design and the representation of the second design.

19. (original) A computer readable storage medium for storing a verification system, comprising:

a set of instructions, the set of instructions when executed implementing a verification process comprising:

receiving a representation of a first design representing a specification having a predetermined functionality;

receiving a representation of a second design, the representation of the second design intended to satisfy the predetermined functionality of the first design, the verification system functioning to affirm that the representation of the second design does in fact satisfy the predetermined functionality of the representation of the first design;

receiving a plurality of design inputs;

comparing the representation of the second design with the representation of the first design, and detecting when the representation of the second design does not satisfy the representation of the first design, the detecting resulting in providing a failure indicator and a characterization of a failure; and

applying one or more constraints to the characterization of the failure, the one or more constraints representing restrictions on permissible test parameters of the second design representation, and determining whether the one or more constraints will prevent the failure from occurring.

20. (original) The computer readable storage medium of claim 19 further comprising:

maintaining the one or more constraints in a list that is applied in an order based upon the characterization of the failure in response to the set of instructions.

21. (original) A verification system, comprising:

a representation of a first design representing a specification having a predetermined functionality;

a representation of a second design, the representation of the second design intended to satisfy the predetermined functionality of the first design, the verification system functioning to affirm that the representation of the second design does in fact satisfy the predetermined functionality of the representation of the first design;

a plurality of design inputs;

a tester for comparing the representation of the second design with the representation of the first design, and detecting when the representation of the second design does not satisfy the representation of the first design, the tester providing a failure indicator and a characterization of a failure in response to the detecting, the tester further comprising:

a symbolic stimulus generator that analyzes the representation of the first design to determine a set of inputs to a test point and generates a set of symbolic stimulus to be applied to corresponding test point inputs in the representation of the second design, the tester accepting as an additional input one or more additional nodes in the first design, finding additional inputs corresponding to the additional nodes, generating a second set of symbolic stimulus from the additional inputs, applying the second set of symbolic stimulus to corresponding inputs in the representation of the second design, and generating an output response for use in verifying functional similarity.

22. (original) The verification system of claim 21 wherein the finding of additional inputs corresponding to the additional nodes comprises tracing from an output-to-input direction through the representation of the first design to identify the additional inputs.

23. (original) The verification system of claim 21 wherein the corresponding inputs in the representation of the second design do not structurally exist in identical form in the representation of the first design, but correspondence in functional result exists.

24. (original) A method of verifying functional similarity between a first design and a second design intended to satisfy functionality of the first design, comprising:

receiving a representation of the first design;

receiving a representation of the second design;

receiving a plurality of design inputs;

comparing the representation of the second design with the representation of the first design, detecting when the representation of the second design does not satisfy the representation of the first design, and providing a failure indicator and a characterization of a failure in response to the detecting;

analyzing with a symbolic stimulus generator the representation of the first design to determine a set of inputs to a test point;

generating a set of symbolic stimulus to be applied to corresponding test point inputs in the representation of the second design;

accepting as an additional input one or more additional nodes in the first design;

finding additional inputs in the first design corresponding to the additional nodes;

generating a second set of symbolic stimulus from the additional inputs; and

applying the second set of symbolic stimulus to corresponding inputs in the representation of the second design and generating an output response for use in verifying functional similarity.

25. (original) The method of claim 24 wherein the finding additional inputs in the first design corresponding to the additional nodes further comprises tracing from an output-to-input direction through the representation of the first design to identify the additional inputs.

26. (original) A computer readable storage medium for storing a verification system, comprising:

a set of instructions, the set of instructions when executed implementing a verification process comprising:

receiving a representation of the first design;

receiving a representation of the second design;

receiving a plurality of design inputs;

comparing the representation of the second design with the representation of the first design, detecting when the representation of the second design does not satisfy the representation of the first design, and providing a failure indicator and a characterization of a failure in response to the detecting;

analyzing with a symbolic stimulus generator the representation of the first design to determine a set of inputs to a test point;

generating a set of symbolic stimulus to be applied to corresponding test point inputs in the representation of the second design;

accepting as an additional input one or more additional nodes in the first design;

finding additional inputs in the first design corresponding to the additional nodes;

generating a second set of symbolic stimulus from the additional inputs; and

applying the second set of symbolic stimulus to corresponding inputs in the representation of the second design and generating an output response for use in verifying functional similarity.